

**Notice of References Cited**

Application/Control No.

09/901,917

Attant(s)/Patent Under

Re-examination  
WALKER ET AL.

Examiner

Toniae M Thomas

Art Unit

2822

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	C	US-5,343,354 B1	08-1994	Lee et al.	361/322
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	N	JP 63-001052 A	01-1988	JP	Kimura et al.	H01L 027/10
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**NON-PATENT DOCUMENTS**

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	U	Wolf et al., "Chemical Vapor Deposition of Amorphous and Polycrystalline Films", <u>Silicon Processing for the VLSI Era - Vol. 1: Process Technology</u> , Lattice Press, 1986, pages 181-182.
	V	Wolf et al., "Semiconductor Memory Process Integration", <u>Silicon Processing for the VLSI Era - Vol. 2: Process Integration</u> , Lattice Press, 1990, page 602.
	W	Wolf et al., "Isolation Technologies for Integrated Circuits", <u>Silicon Processing for the VLSI Era - Vol. 2: Process Integration</u> , Lattice Press, 1990, page 48.
	X	Wolf et al., "Hot Carrier-Resistant Processing and Device Structures", <u>Silicon Processing for the VLSI Era - Vol. 3: The Submicron MOSFET</u> , Lattice Press, 1995, pages 634-636.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.